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## **New CMOS technologies restrict high-performance A/D-converters for LTE and multi-carrier WCDMA**

***ADMS Design has analyzed what combinations of bandwidth and resolution you can expect in different CMOS technologies – so called process nodes. While each new CMOS node provides faster transistors, the available dynamic range is also reduced in the signal path. At any given resolution, there is an upper limit to the A/D-converter bandwidth achievable while maintaining reasonable power dissipation. That upper limit to bandwidth is technology-dependent, and is lower for each new CMOS node. The results have direct consequences for A/D-converters used in LTE and multi-carrier WCDMA infrastructure. The study will be presented at the Nordic microelectronics conference NORCHIP in November.***

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Dr. Bengt Jonsson, founder of ADMS Design AB, will present parts of the company research during the Nordic microelectronics conference NORCHIP in November. The conference contribution analyzes how technology scaling limits practically achievable performance for CMOS analog-to-digital converters, and is based on measured performance data reported in over 1100 scientific papers between 1976 and 2010.

“This will be interesting to discuss with other scientists and companies”, says Bengt Jonsson. “Our results have direct implications for A/D-converters such as those required for LTE and multi-carrier WCDMA infrastructure, which is shown in the study. Even if performance can be increased somewhat by accepting increased power dissipation, the results show that ADC manufacturers will have to use quite old technology or extra process options in order to have a chance to reach the combinations of bandwidth and resolution required in these systems. The possibility for future integration of A/D-converters with digital ASIC parts is therefore seriously challenged. A more likely scenario is therefore integration with RF/IF or to put two chips in the same package.”

“As far as we are aware, this is the first larger study of how measured actual performance correlate with CMOS technology. Other studies have focused on performance evolution over time, but that is not the same thing since a particular CMOS node can have a publication lifespan of more than 10 years. Correlation with time is therefore weak.”

The study is part of a larger ongoing project at ADMS Design where the results are continuously integrated into the *Experience-based Design Optimization* services offered by the company.

NORCHIP web page (<http://www.norchip.org>)

NORCHIP Program (<http://www.norchip.org/CHIP10.pdf>)

PRESS RELEASE

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